26.8 A 1.9GHz Single-Chip CMOS PHS Cellphone

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The personal handy-phone system (PHS), which was first commercially launched in Japan in 1995, has enjoyed a recent resurgence in China with over 50 million subscribers in 2004 [1]. In this paper, a radio SoC that incorporates all functions of a PHS cellphone in a 0.18μm CMOS technology is presented. The solution is a cellphone SoC in volume production. As shown in Fig. 26.8.1, the analog/RF portion contains a PHS transceiver, audio/voice-band data converters as well as amplifiers for microphone, earpiece, and speaker. The digital circuits include a PHS Modem, PHS TDMA, ARM9 CPU, voice subsystem, as well as various interfaces to memory, LCD, keyboard, and WLAN. The single-chip cellphone provides a low-cost small-form factor solution that simplifies the board assembly.

PHS is a TDMA/TDD system that employs π/4 QPSK modulation with 300kHz bandwidth and operates in the 1880.15 to 1929.65MHz frequency band. Figure 26.8.2 shows a block diagram of the PHS transceiver, consisting of a frequency synthesizer, a linear receiver, and a linear transmitter. This radio uses a direct-conversion architecture with a VCO operating at twice the RF signal. Choosing a VCO frequency at twice the RF signal frequency is advantageous because 1) frequency pulling by the transmitter is weaker, 2) the size of on-chip spiral inductor is smaller, and 3) the quadrature LO_{RF} can be easily generated with a divide-by-two circuit.

A key challenge in the design of the frequency synthesizer is to support *seamless handover* between cellular base stations, which requires fast synthesizer settling [1]. The measured results in Fig. 26.8.3 show that the fractional-N synthesizer with a 3rd-order 3b ΔΣ modulator achieves a 15μs settling time. The VCO is based on an LC resonant tank with a diode varactor. An array of switchable capacitors is used to ensure that the VCO frequency can support the entire PHS band at all operating temperatures and process corners. The synthesizer has a 120kHz loop bandwidth to meet both phase noise and settling time requirements. The loop bandwidth can be adjusted during channel switching to speed up the transient response [2]. In addition, the reverse bias voltage on the VCO varactor is confined to a small range of 200mV to provide accurate control of the VCO gain (K_{VCO}). The synthesizer phase noise measured at the transmitter output, shown in Fig. 26.8.4, is -98dBc/Hz at 100kHz offset (dominated by reference-clock phase noise) and -118dBc/Hz at 600kHz (dominated by ΔΣ quantization noise). The synthesizer, including the LO buffer, consumes 25mA.

As illustrated in Fig. 26.8.2, the receiver converts the incoming RF signal to quadrature baseband outputs while providing enough gain and blocker attenuation for proper demodulation of the desired signal. The LNA consists of a cascoded differential pair with inductive degeneration and inductive loading. The LNA has an adjustable RF gain to accommodate RF input signals as large as -5dBm. Subsequent RF gain stages provide additional gain, as well as gain steps for AGC. The AGC is further aided through the use of on-chip envelope detectors at the output of the RF stages. As shown in Fig. 26.8.5, down conversion is performed by passive in-phase (I) and quadrature (Q) mixers implemented with NMOS native devices. The common-mode voltage and the amplitude of LO_{RF} signal that strongly influence the gain of the passive mixer, are generated by a two-stage LO buffer without bulky inductors. A replica bias circuit in the common-mode feedback of the LO buffer sets the V_{GS} of the passive mixer devices, M6-M9, at the edge of conduction. The output of the mixer is low-pass filtered by a programmable-gain, active-RC 2nd-order Butterworth filter with 17dB attenuation at 600kHz. DC offset is cancelled at the output of the mixer by an offset DAC. The filtered analog baseband signals are quantized by a pair of 2nd-order ΔΣ ADCs. These ADCs have an 80dB dynamic range to accommodate large blockers that can be easily attenuated digitally. The measured receive chain NF is 3.5dB. The overall receiver sensitivity is -106dBm (including loss due to an off-chip transmit/receive switch) and the receiver meets the PHS alternate channel blocker specification of +51dB. The entire receiver draws 32mA.

In the transmitter, the digital baseband signal is up-converted by two 9b 38.4MS/s current-steering DACs into I and Q baseband currents. Because of the high sampling frequency, no explicit low-pass filtering is needed to remove DAC spectral images. An inductorless LO buffer, similar to that in Fig. 26.8.5, is used to generate the LO signals for a pair of active transmit mixers that convert the baseband currents directly to 1.9GHz. An RF VGA preceding the power amplifier (PA) helps compensate for gain variation over process and temperature. The PA output stage consists of four cascoded amplifiers in parallel to enable power-efficient adjustment of gain and output power. Turning off one of the cascoded amplifiers by grounding the gate of its cascode transistor can result in large V_{DG} stress if a large voltage swing is present at the output drain node. In this design, each cascoded amplifier is enabled by a switch in series with ground to avoid reliability concerns. The transmitter draws 29mA and has an rms EVM of 4% at +1dBm output power, and an adjacent channel power rejection (ACPR) at 600kHz of -59dBc.

The integration of both analog and digital circuits enables the use of digital signal processing to overcome analog and RF impairments and thereby reduce power and area for analog and RF circuits as well as improve overall wafer yield [3]. In this design, an RF loop-back path is provided from the transmit RF VGA to the receiver, as shown in Fig. 26.8.2. This loop-back mode allows the receiver filter bandwidth and transmitter carrier leak to be calibrated, reducing the device matching requirements.

Figure 26.8.6 shows the die micrograph of the single-chip PHS cellphone. It occupies a total die area of 35mm^2 in a standard 0.18μm CMOS technology with a 3.0V I/O supply internally regulated to 1.8V for core devices. The cellphone based on this IC, packaged in a 276-pin BGA, is fully functional with seamless handover and has passed all regulatory certifications. The measured performance of the radio is summarized in Fig. 26.8.7.

Acknowledgment:
The design of a cellphone SoC requires significant amount of resources beyond that of the RF and analog IC design team. The authors wish to acknowledge the contributions of the entire PHS team at Atheros, especially their efforts in algorithm development, digital design, and system design and verification.

References:
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[3] S. Mehta, et al, “An 802.11g WLAN SoC,” *ISSCC Dig. Tech. Papers*, pp. 94-95, Feb., 2005.

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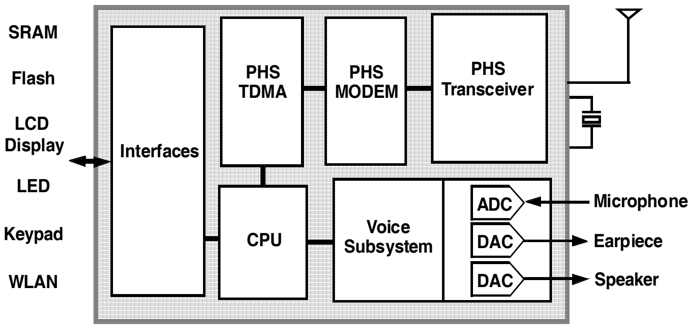

Figure 26.8.1: Block diagram of the single-chip PHS cellphone.

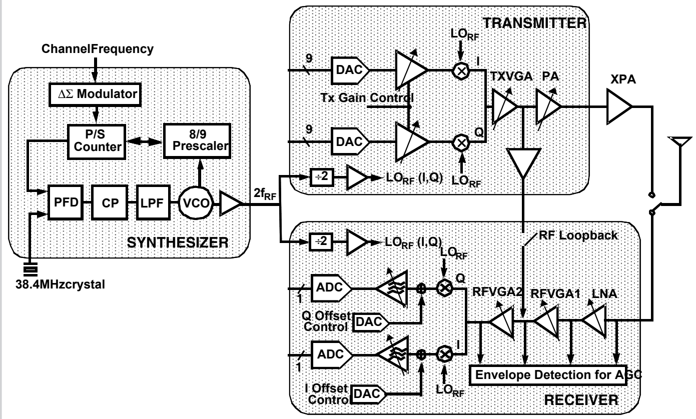

Figure 26.8.2: Block diagram of CMOS RF PHS transceiver.

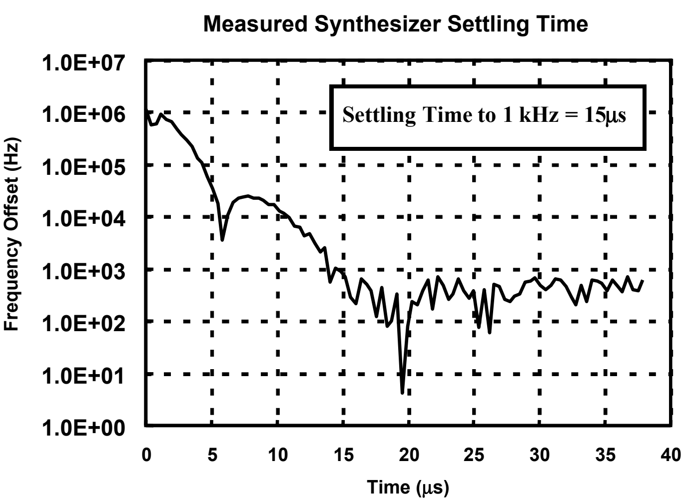

Figure 26.8.3: Measured synthesizer settling time from 1895.15 to 1917.95MHz.

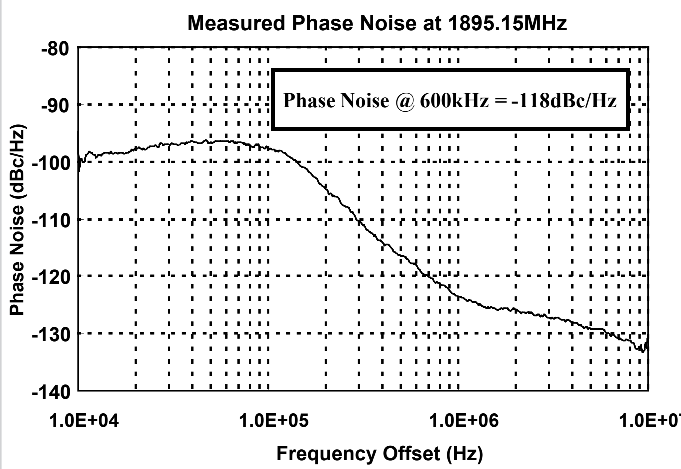

Figure 26.8.4: Measured synthesizer phase noise at 1895.15MHz.

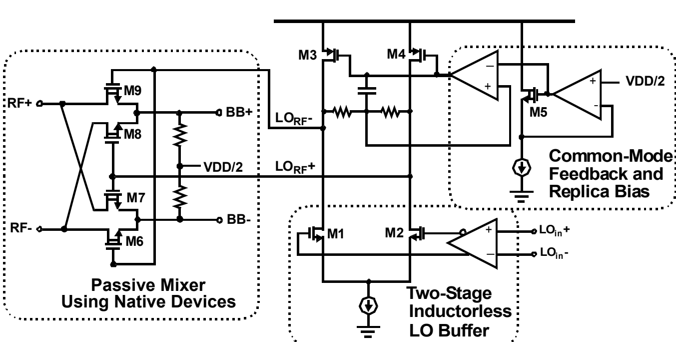

Figure 26.8.5: Schematic of receive mixer and LO buffers.

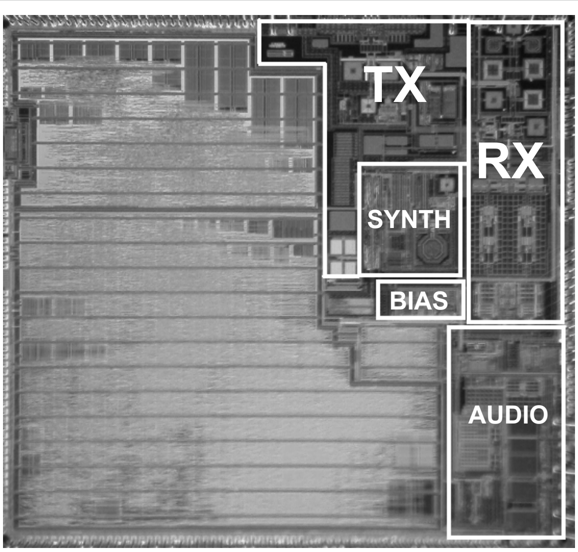

Figure 26.8.6: Chip micrograph of the single-chip PHS cellphone.

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Performance Summary

Power Dissipation	
RF Transmitter	29mA
RF Receiver	32mA
RF Synthesizer	25mA
Talk Mode (1/8 duty cycle Tx & Rx)	81mA (including audio and digital)
Standby Mode	1mA (including audio and digital)
Phase Noise @ 1.9GHz	-118dBc/Hz @ 600kHz offset
Settling time to +/- 1kHz	15µs
Receive Sensitivity	-106dBm
Receiver Noise Figure	3.5dB
Transmit Power (EVM compliant)	+4 dBm
Transmit EVM @ +1dBm	4% rms
Technology	Standard 0.18µm CMOS
Die Size: Total	35 mm^2
Radio and Analog	12 mm^2
Package	276-pin BGA

Figure 26.8.7: Summary of measured performance.